

Fig. 1

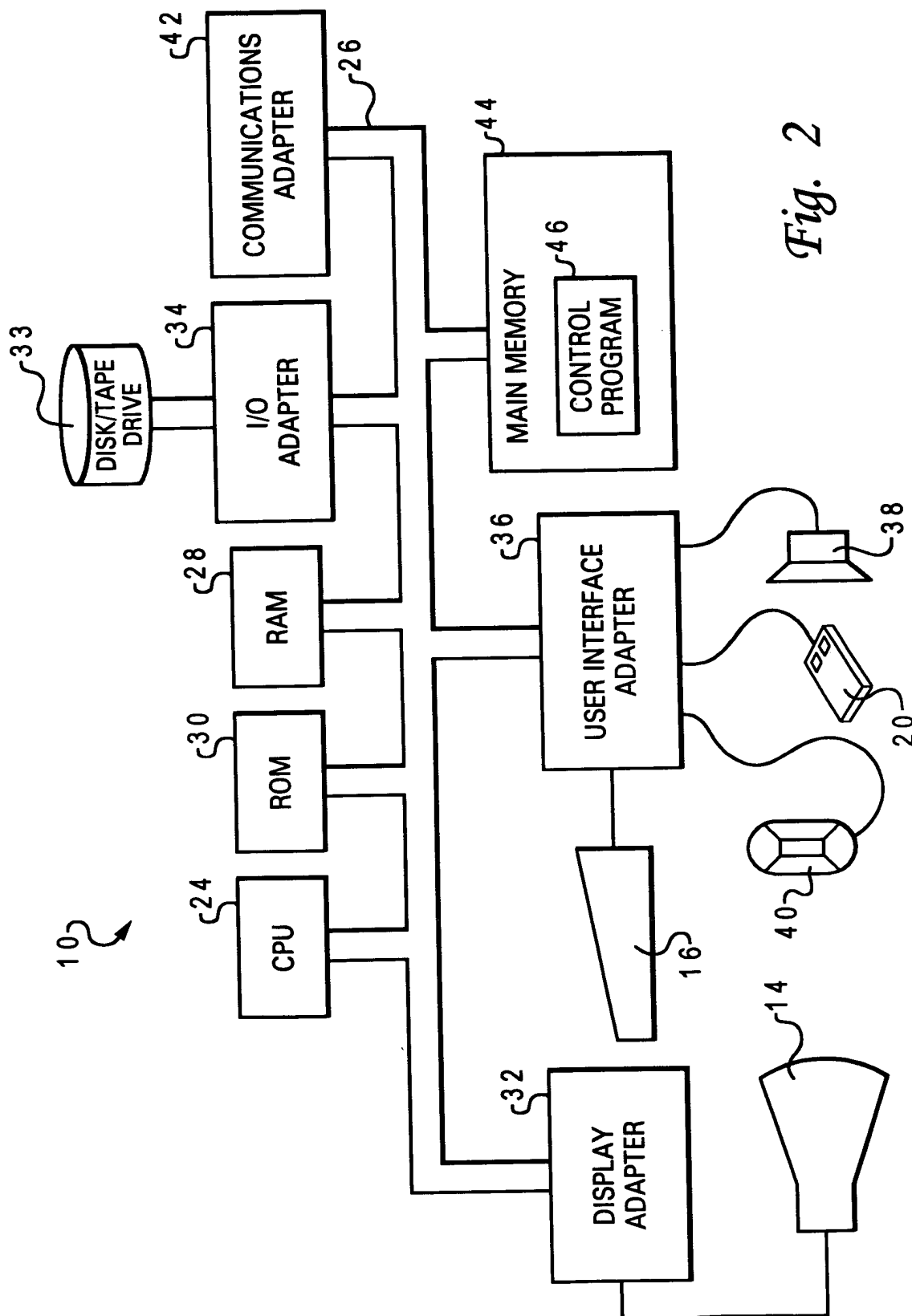
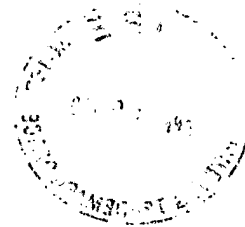


Fig. 2

FIG. 2

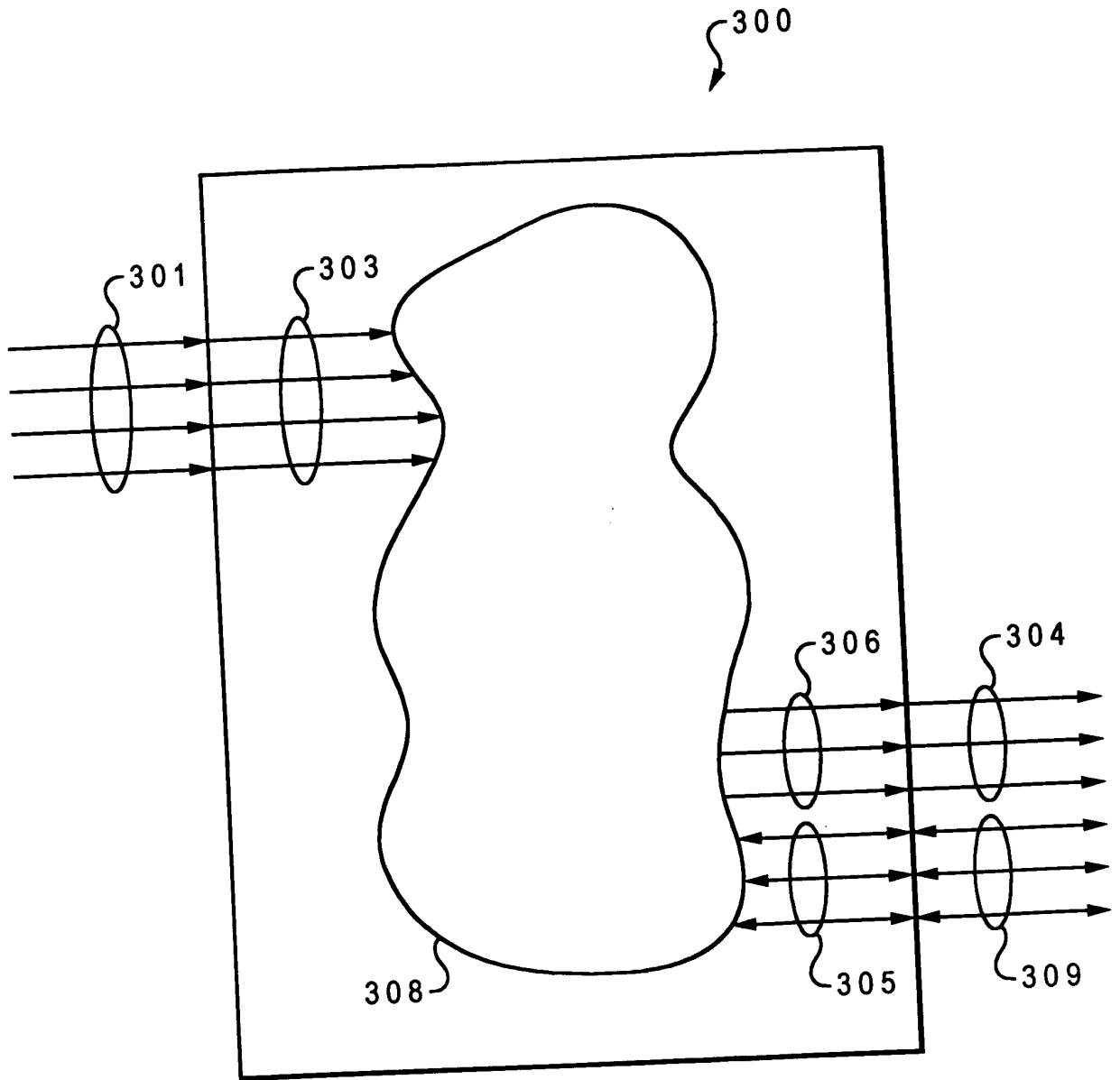


Fig. 3A

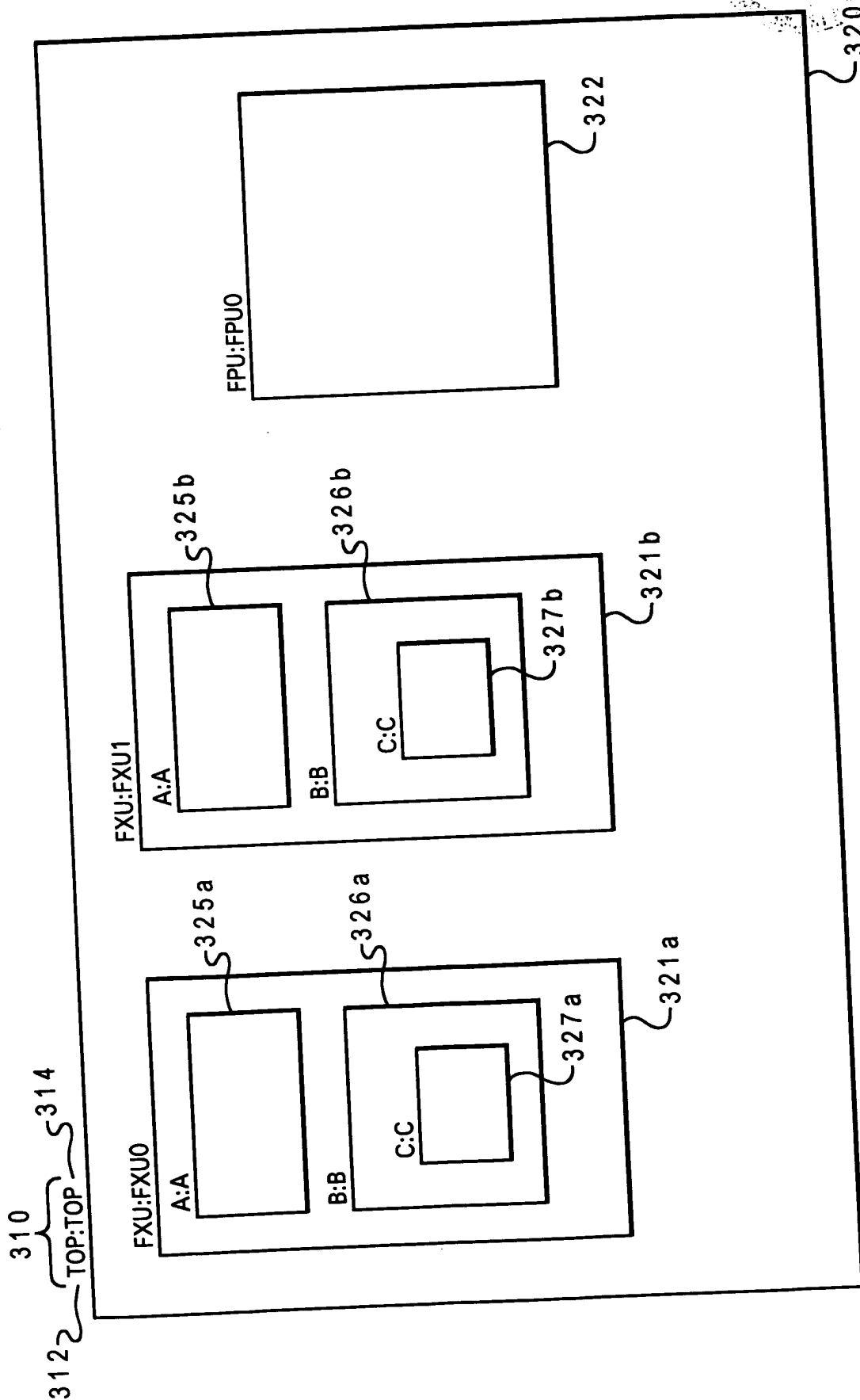
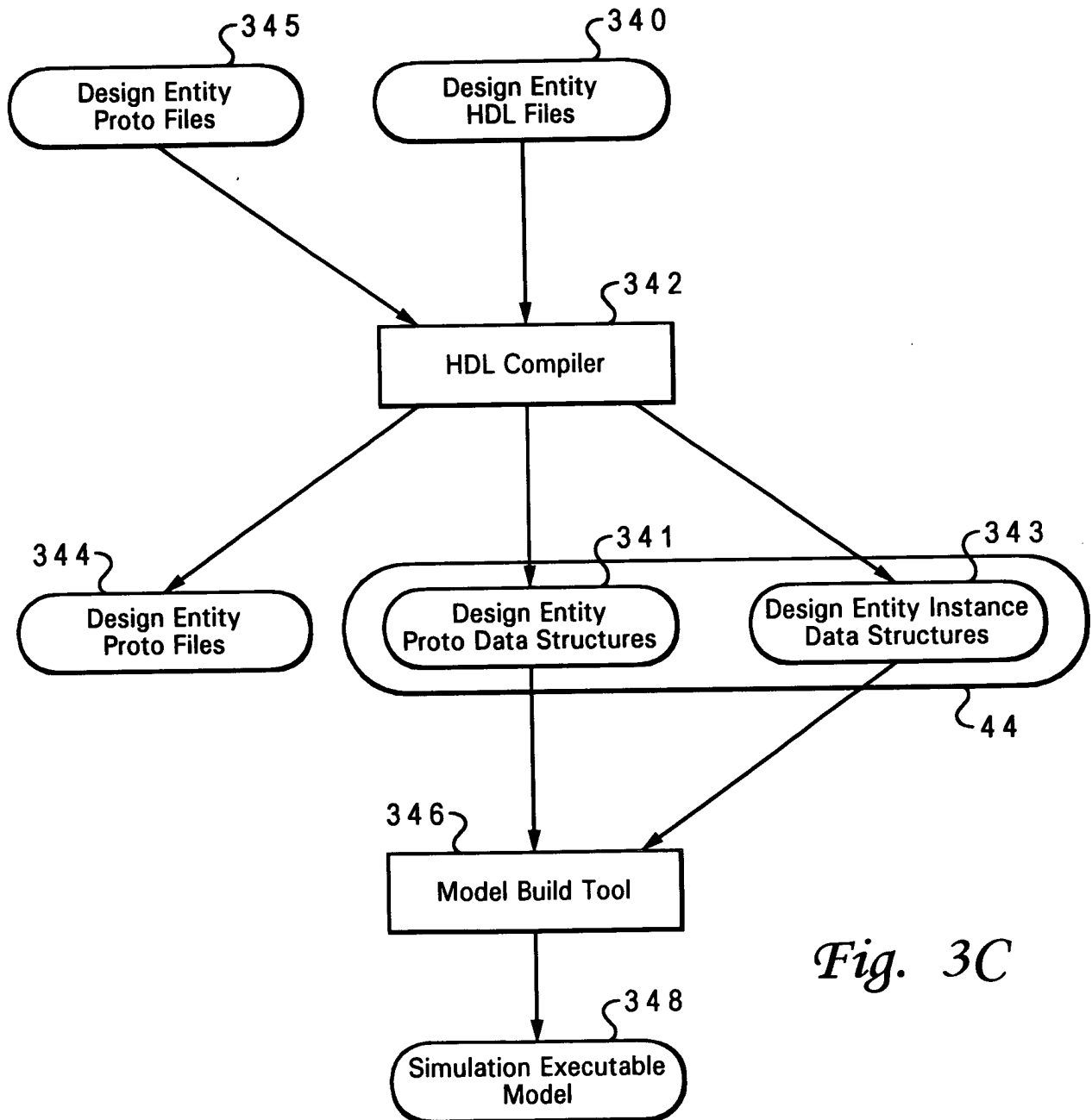


Fig. 3B

*Fig. 3C*

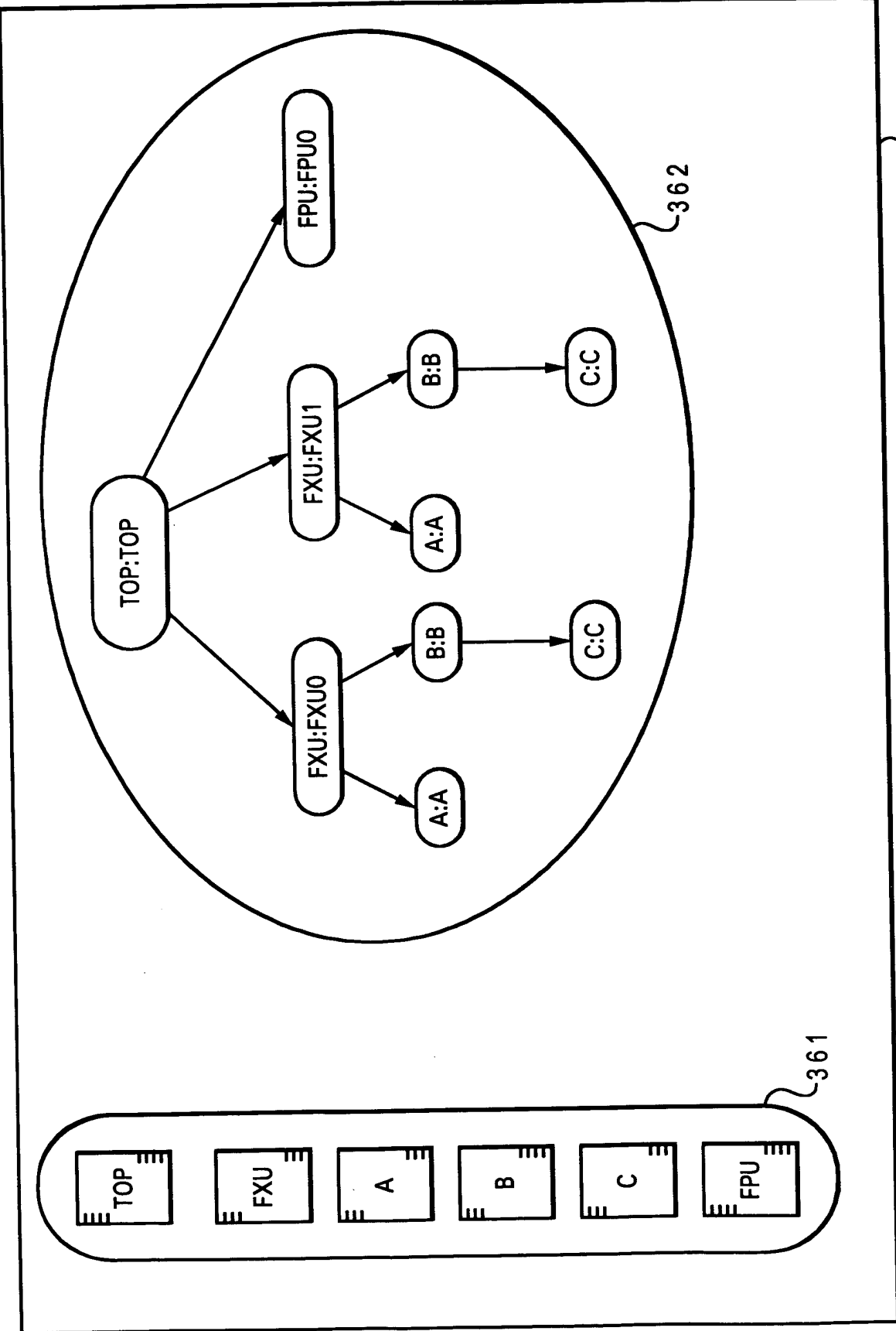


Fig. 3D

FIG. 3D

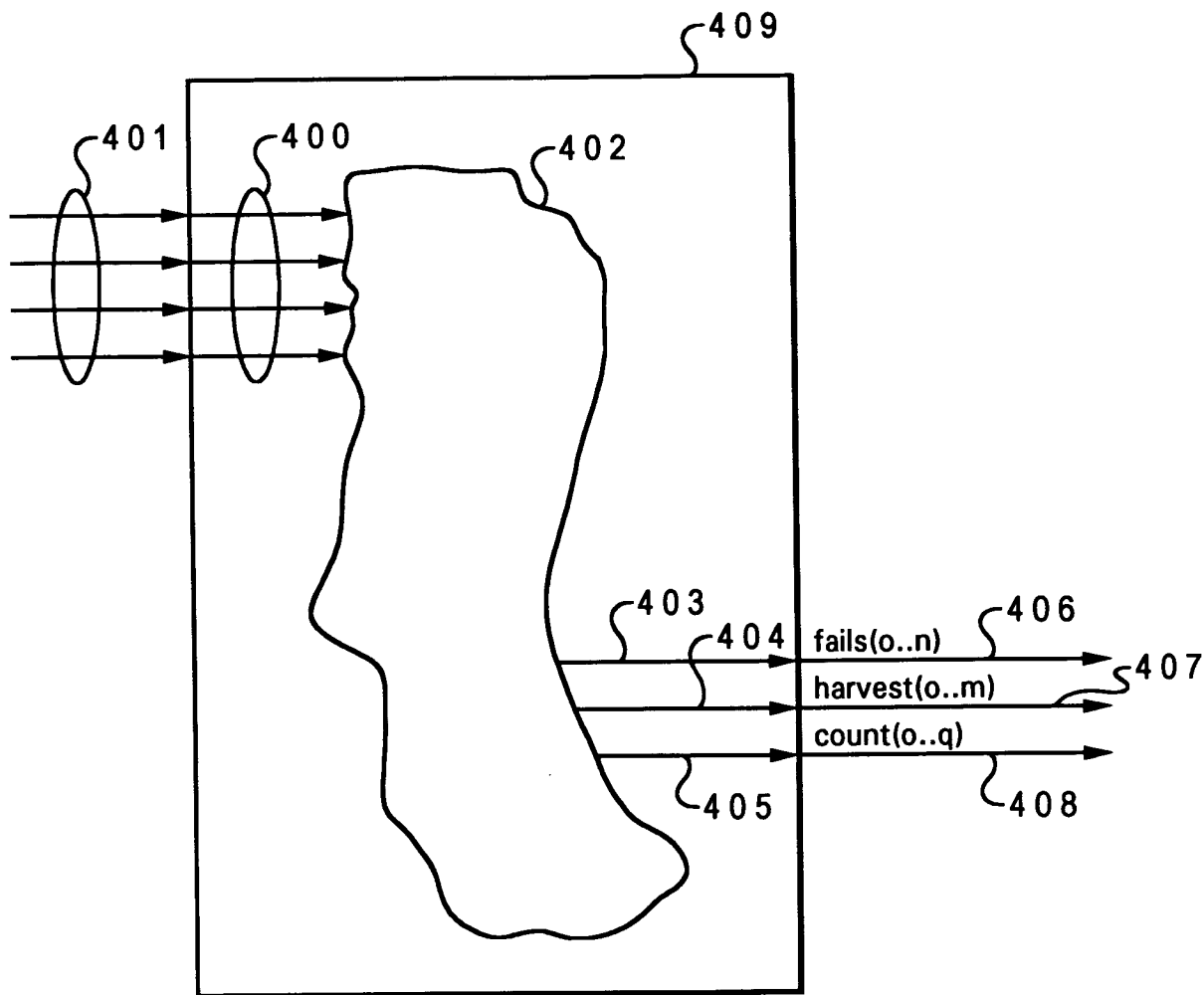


Fig. 4A

FIG. 4A

TOP:TOP

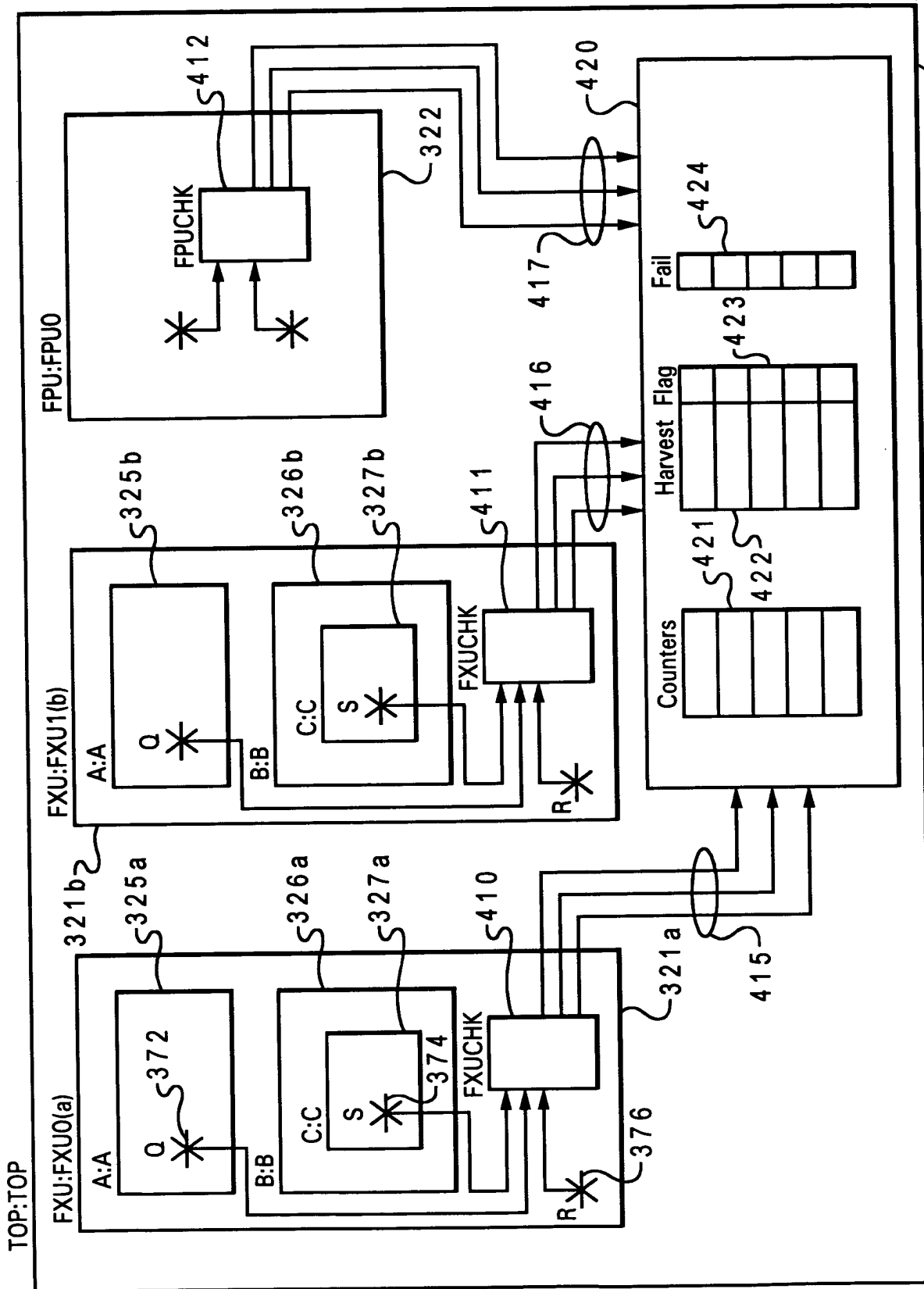


Fig. 4B



ENTITY FXUCHK IS

```

PORT(  S_IN      :    IN std_ulogic;
        Q_IN      :    IN std_ulogic;
        R_IN      :    IN std_ulogic;
        clock     :    IN std_ulogic;
        fails     :    OUT std_ulogic_vector(0 to 1);
        counts    :    OUT std_ulogic_vector(0 to 2);
        harvests  :    OUT std_ulogic_vector(0 to 1);
);

```

4 5 0

4 5 2 { --!! BEGIN  
--!! Design Entity: FXU;

4 5 3 { --!! Inputs  
--!! S\_IN => B.C.S;  
--!! Q\_IN => A.Q;  
--!! R\_IN => R;  
--!! CLOCK => clock;  
--!! End Inputs

4 5 4 { --!! Fail Outputs;  
--!! 0 : "Fail message for failure event 0";  
--!! 1 : "Fail message for failure event 1";  
--!! End Fail Outputs;

4 5 5 { --!! Count Outputs;  
--!! 0 : <event0> clock;  
--!! 1 : <event1> clock;  
--!! 2 : <event2> clock;  
--!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;  
--!! 0 : "Message for harvest event 0";  
--!! 1 : "Message for harvest event 1";  
--!! End Harvest Outputs;

4 5 7 { --!! End;

4 5 1

4 4 0

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

4 5 8

*Fig. 4C*

2025-09-10 10:00:00

10/33

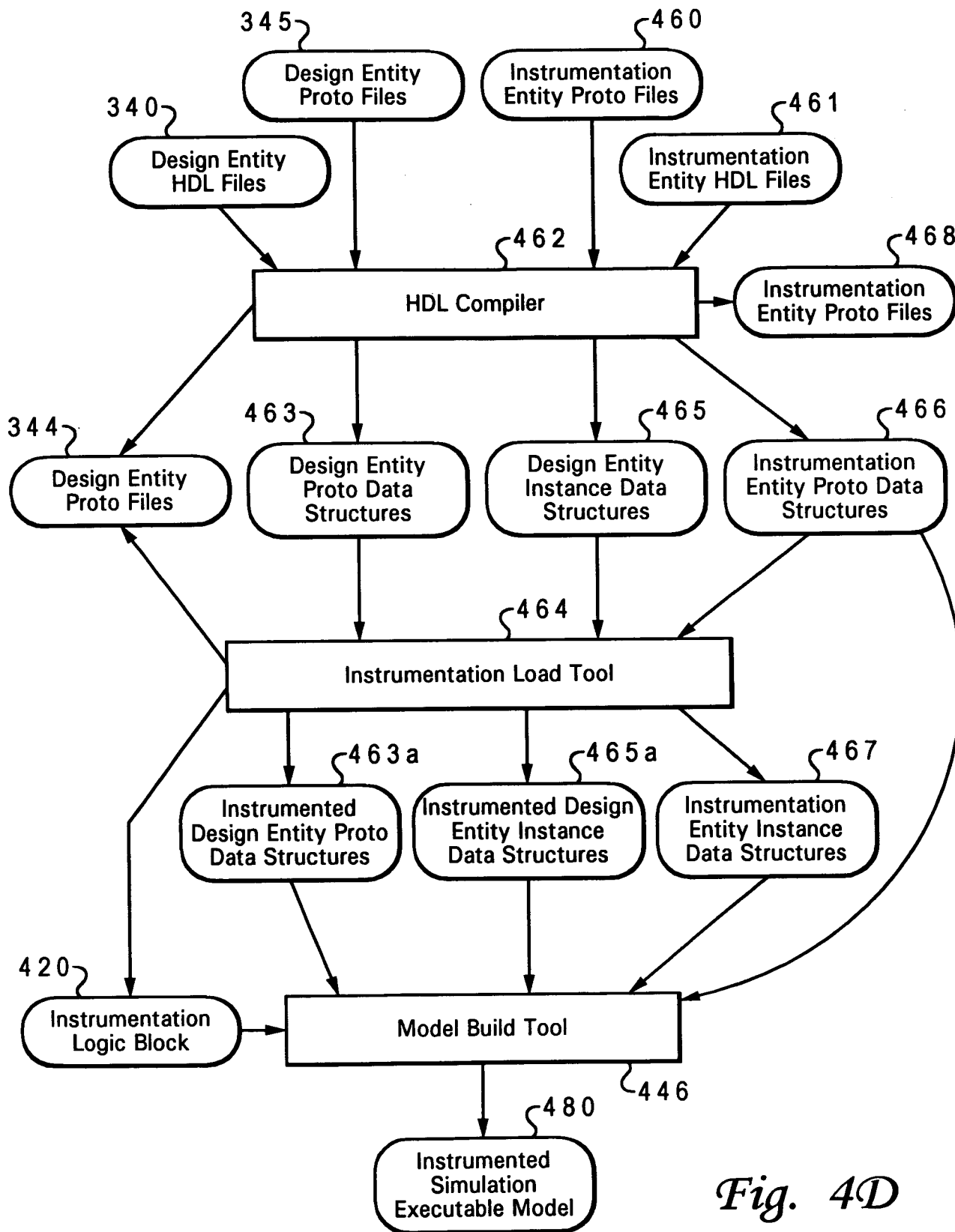


Fig. 4D

FIG. 4E

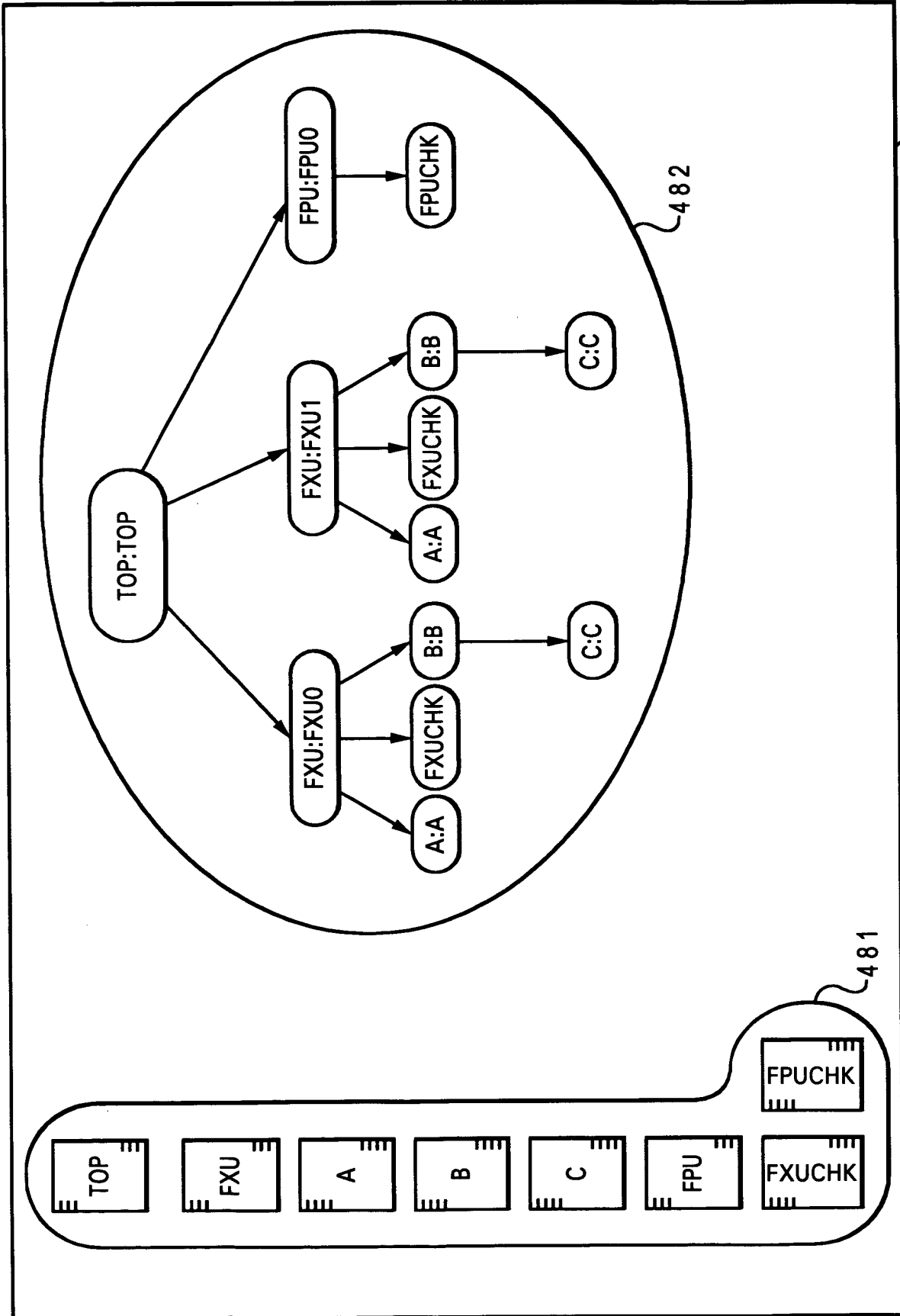


Fig. 4E

FIG. 5A

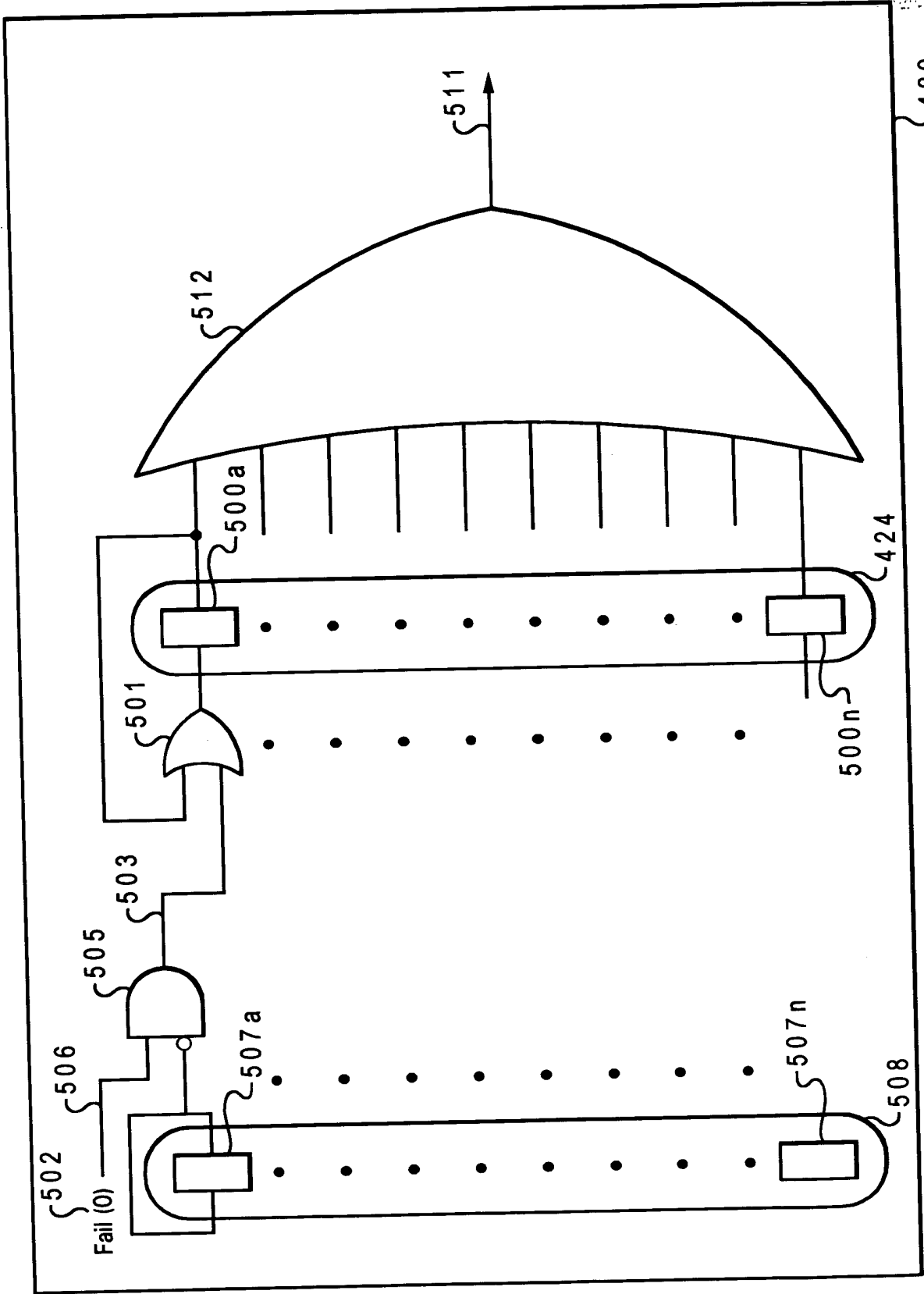


Fig. 5A



FIG. 5B

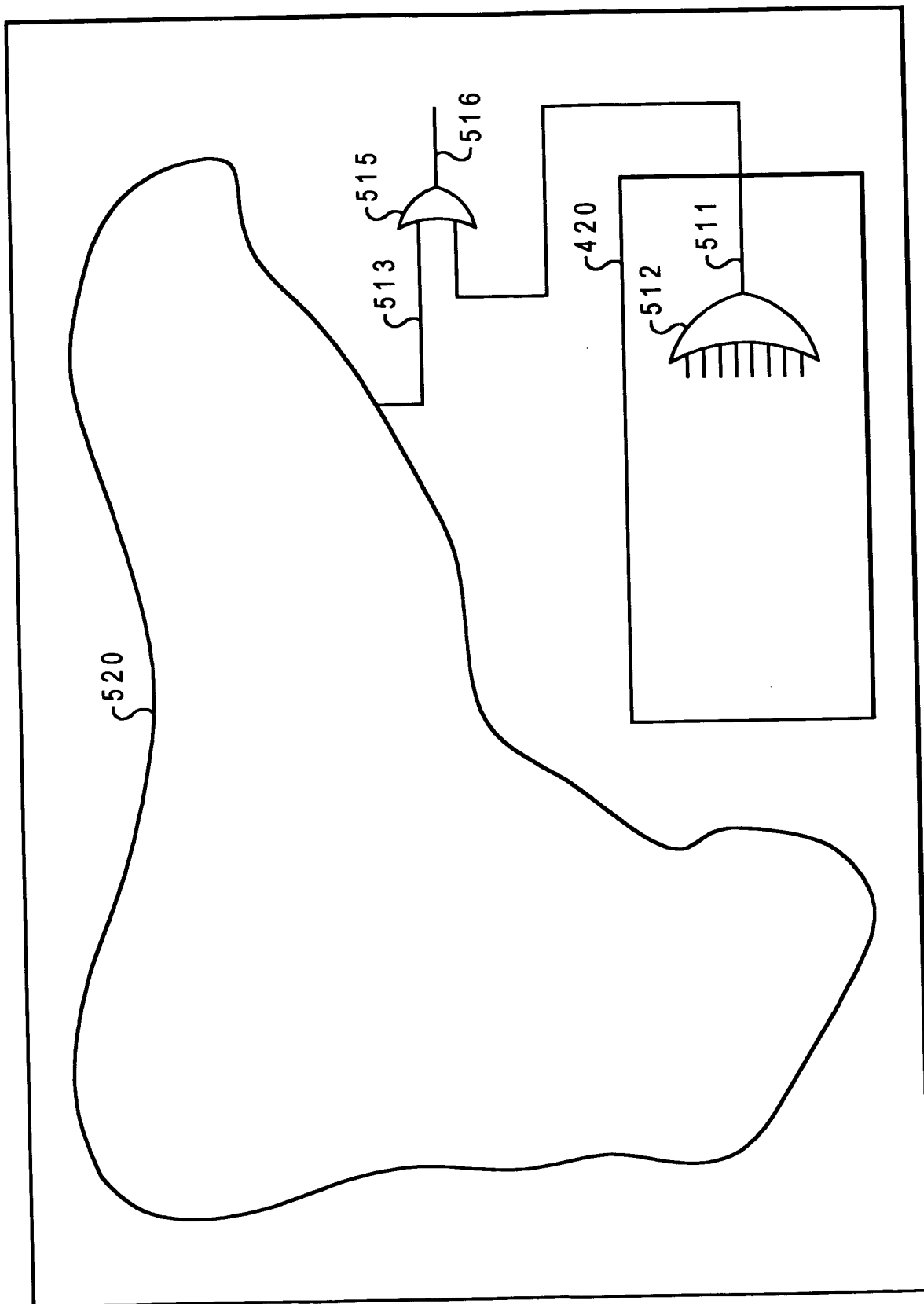


Fig. 5B

FIG. 6A

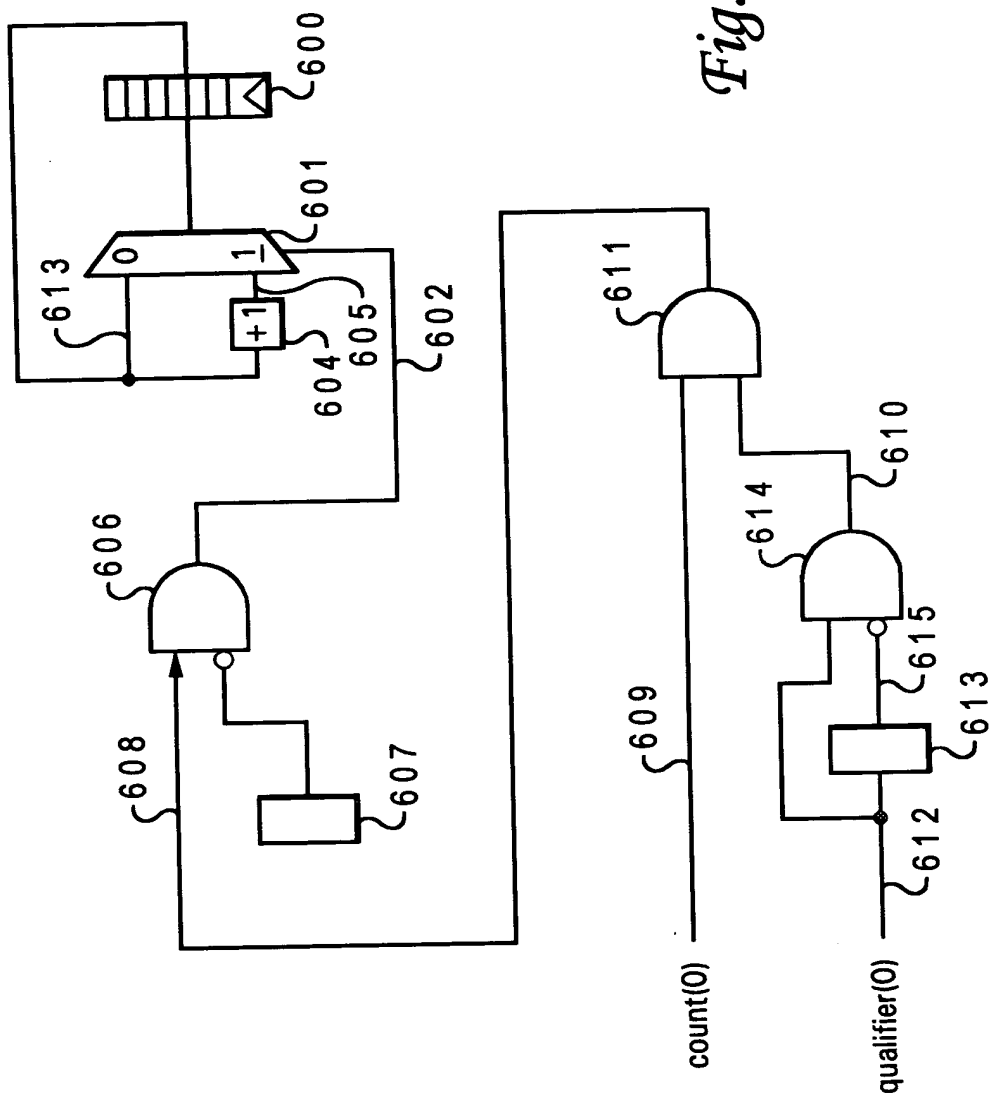


Fig. 6A

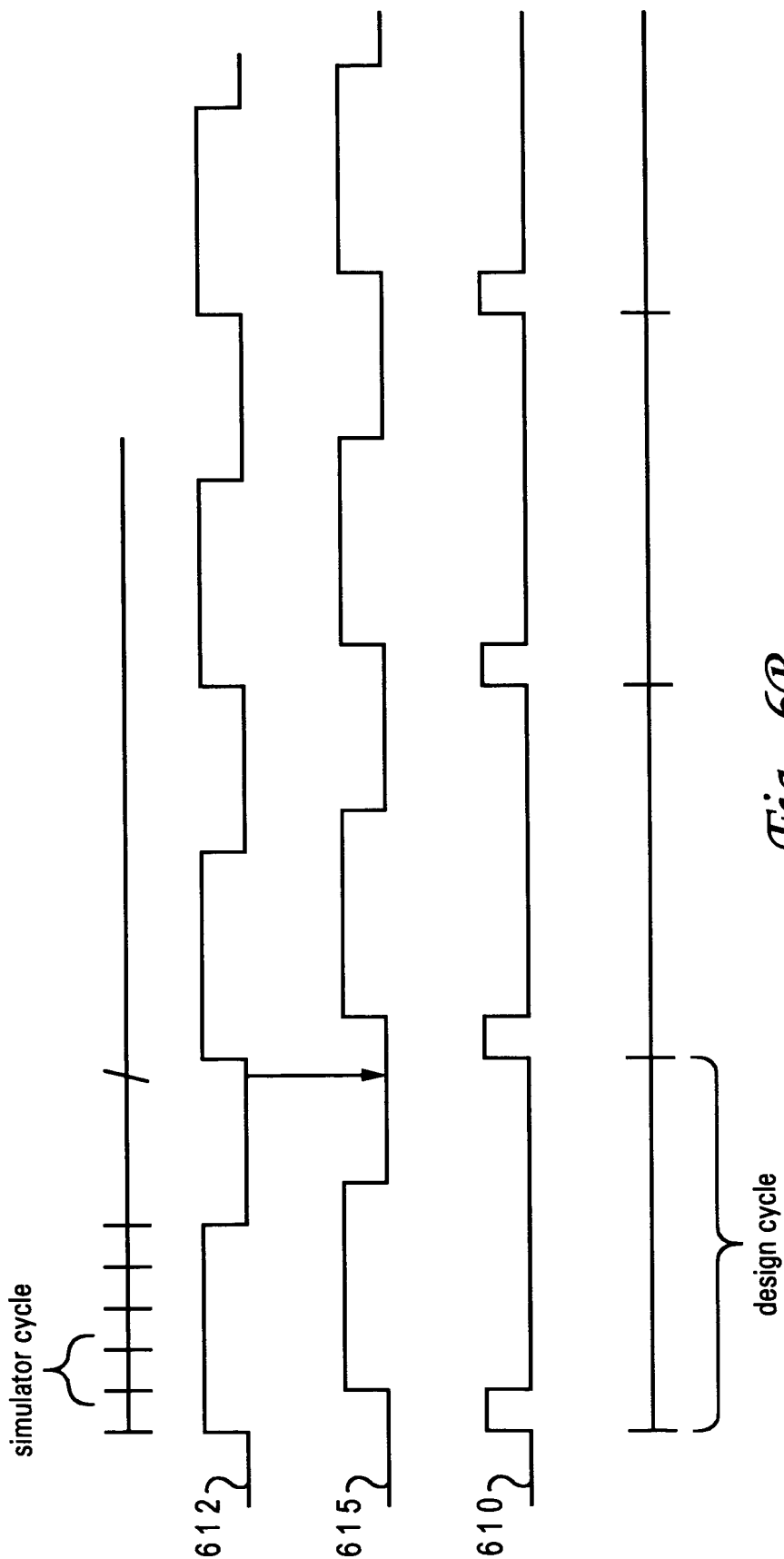


Fig. 6B

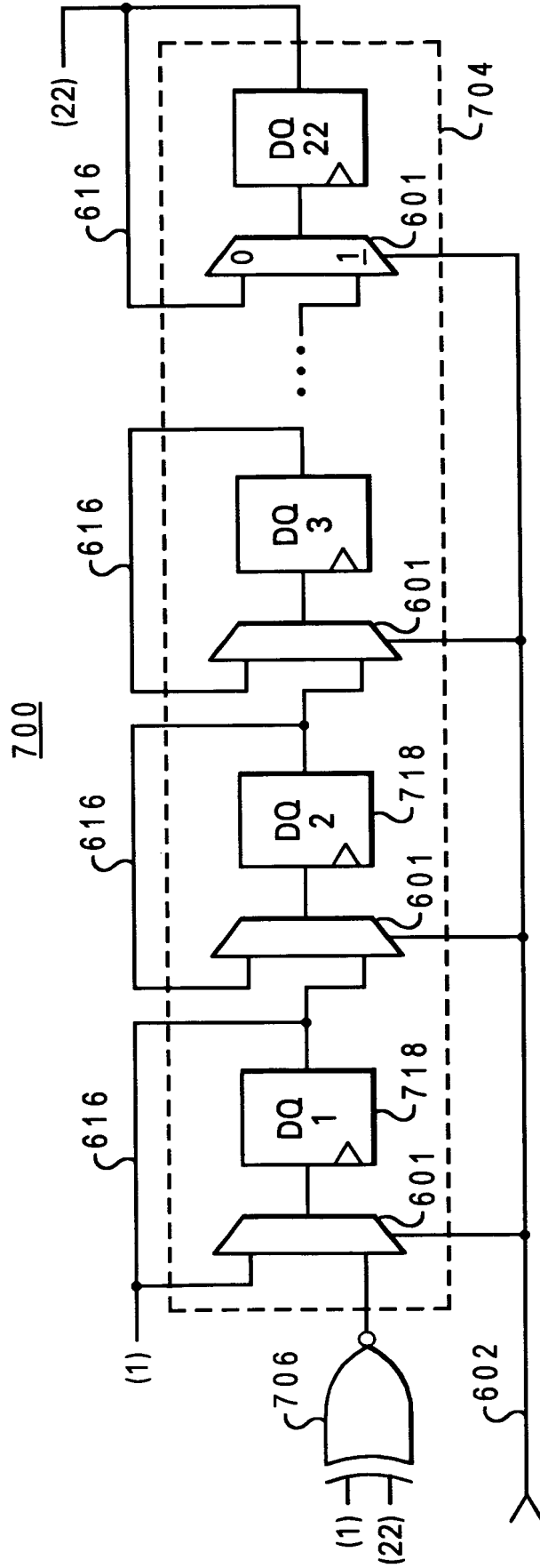
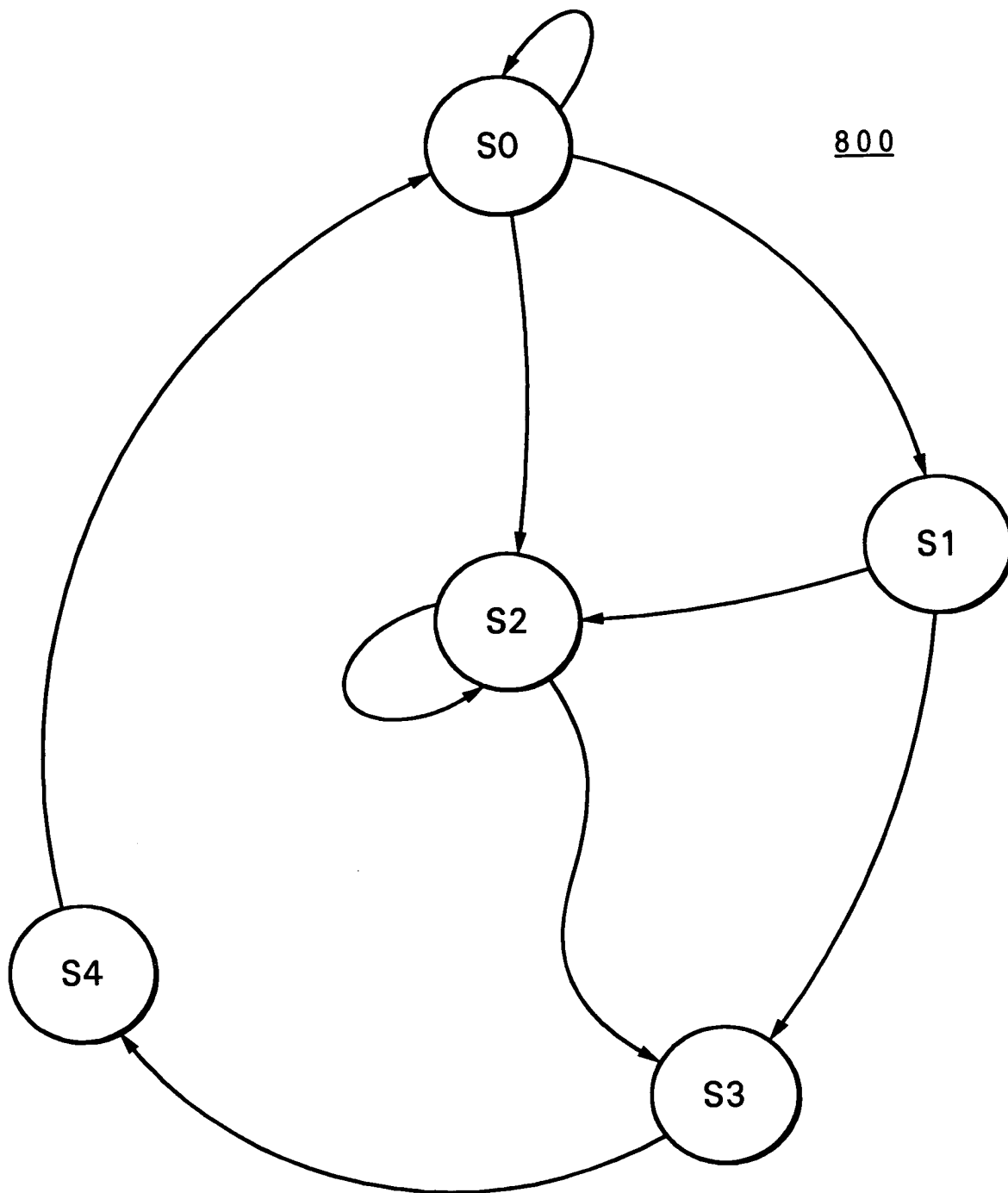


Fig. 7

800

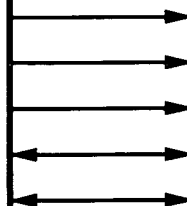
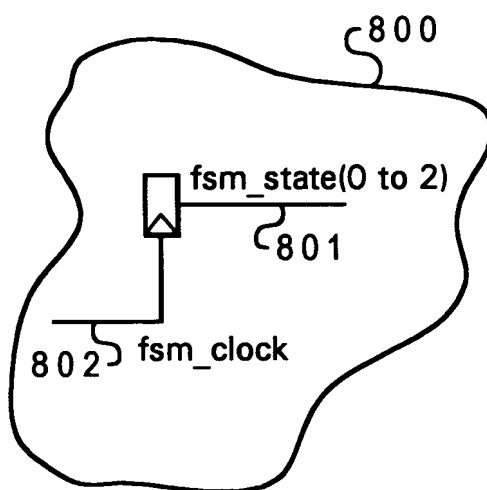
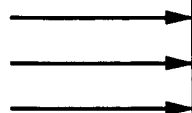
*Fig. 8A*  
*Prior Art*

T00010-25225/50



entity FSM : FSM

850



*Fig. 8B*  
*Prior Art*

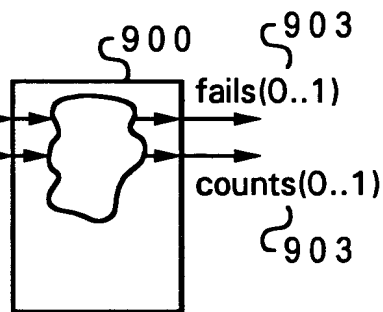
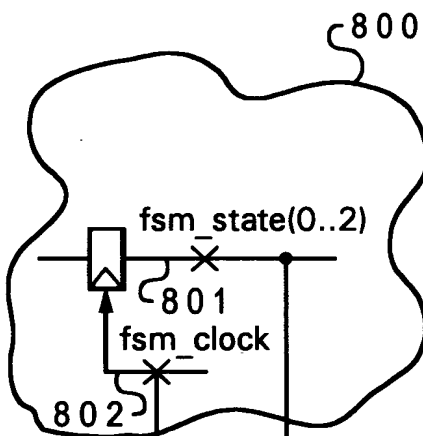
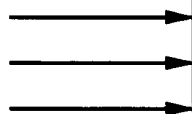
*Fig. 8C*

$$-852 \} 860$$



entity FSM : FSM

850



\$examplefsm : \$examplefsm

902

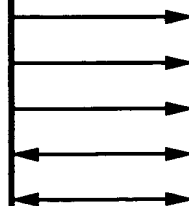
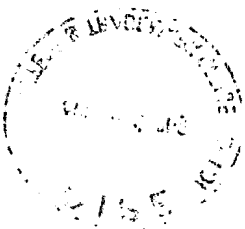
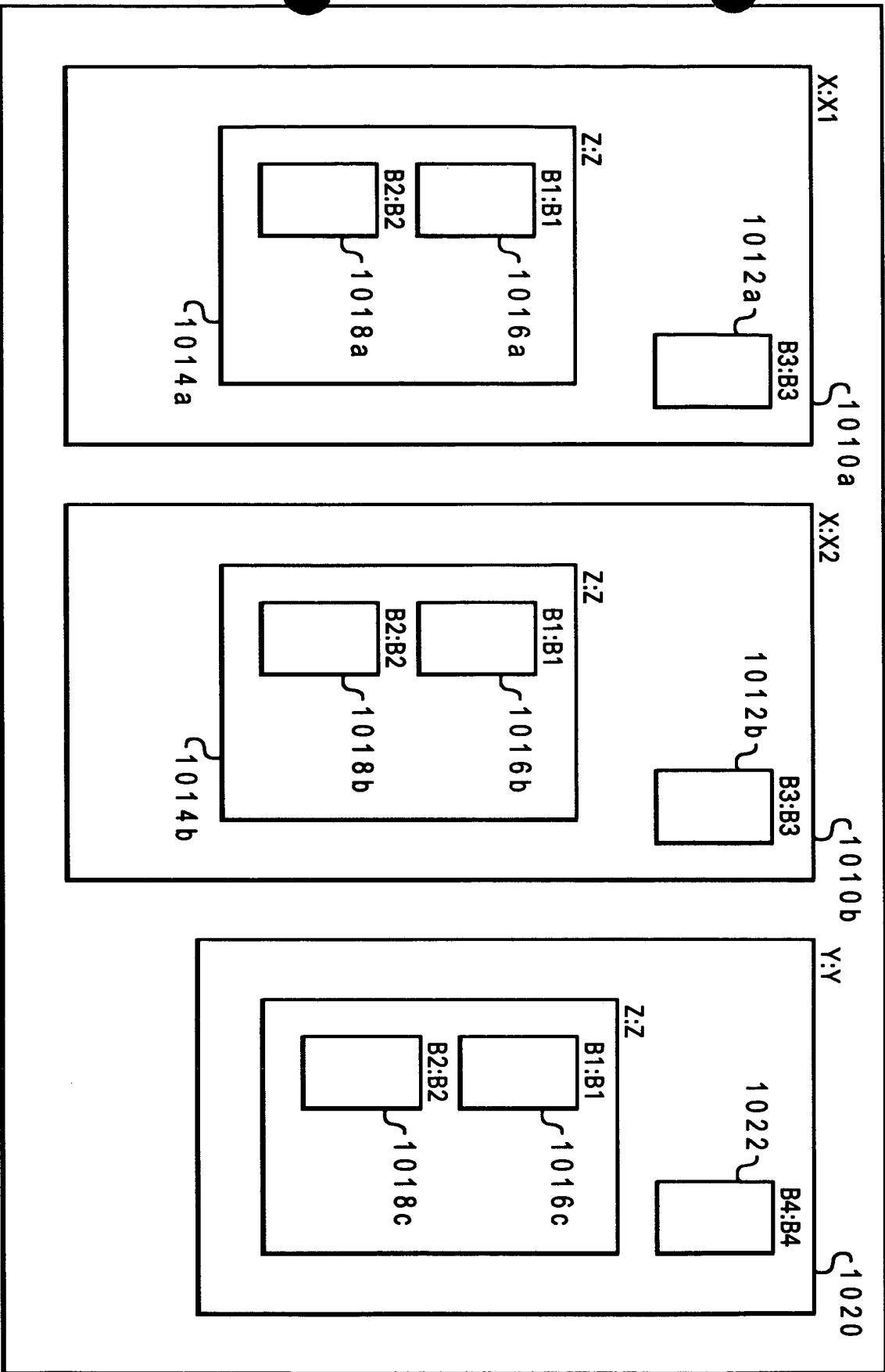


Fig. 9



TOP:TOP

Fig. 10A



09752252-040904



Fig. 10B

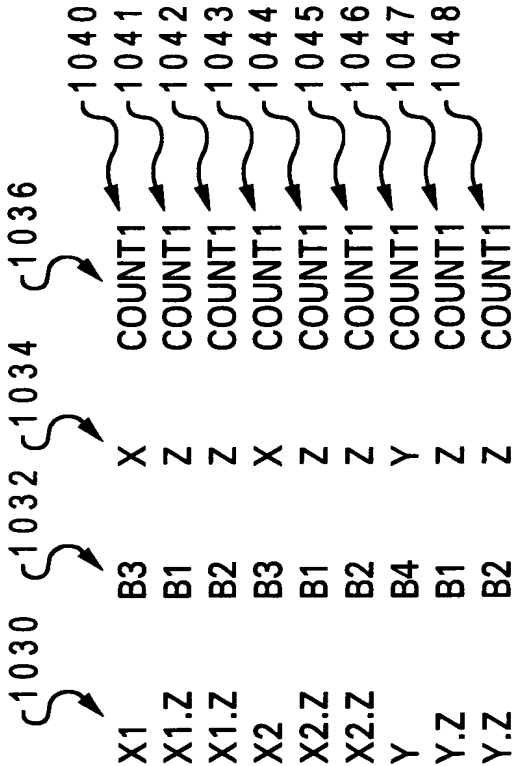
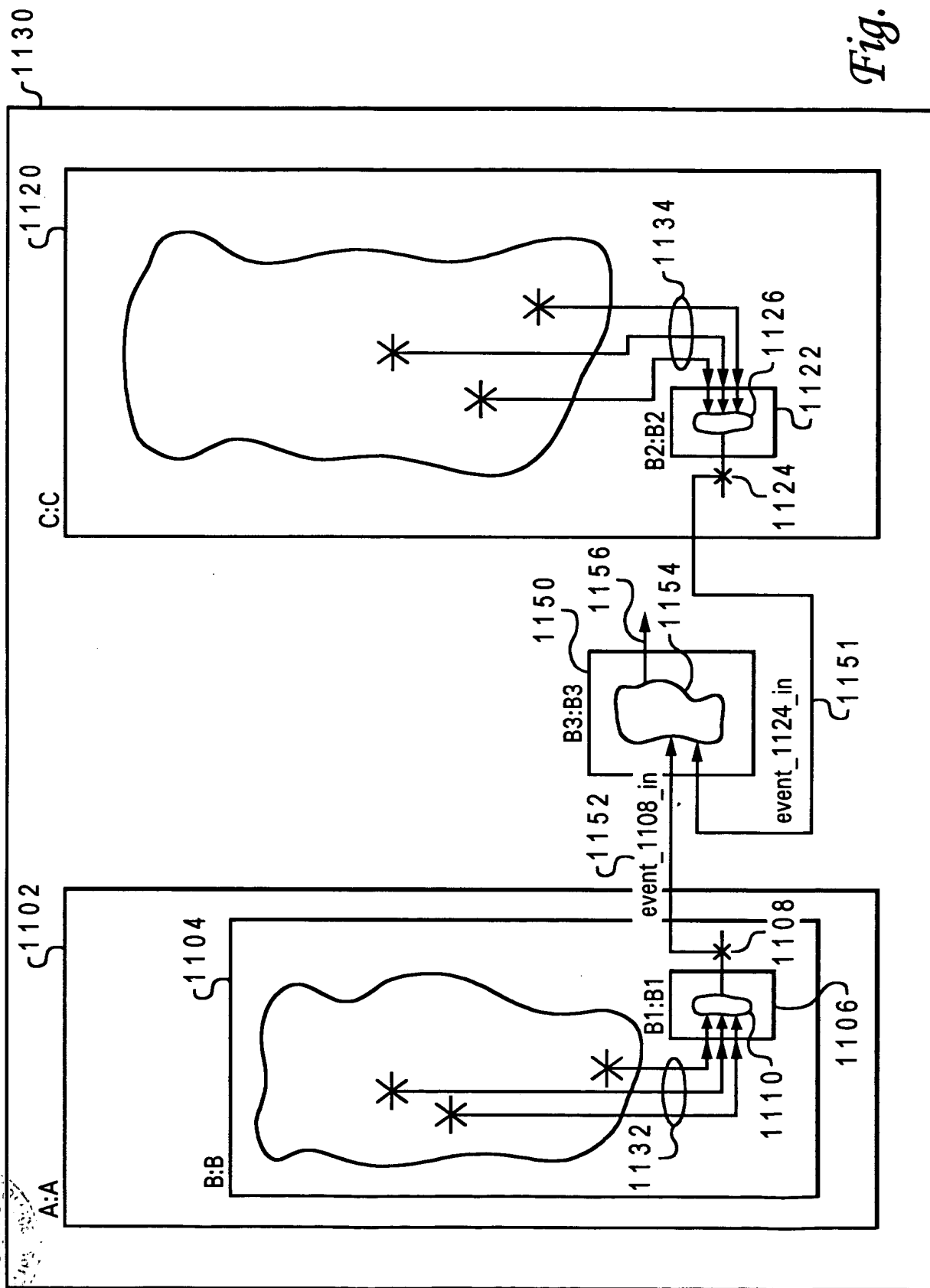


Fig. 10C



Fig. 10D

Fig. 11A



TOP:TOP





--!! Inputs  
--!! event\_1108\_in <= C.[B2.count.event\_1108];  
--!! event\_1124\_in <= A.B.[B1.count.event\_1124];  
--!! End Inputs

1163 } 1165 } 1161 }  
1164 } 1166 } 1162 }

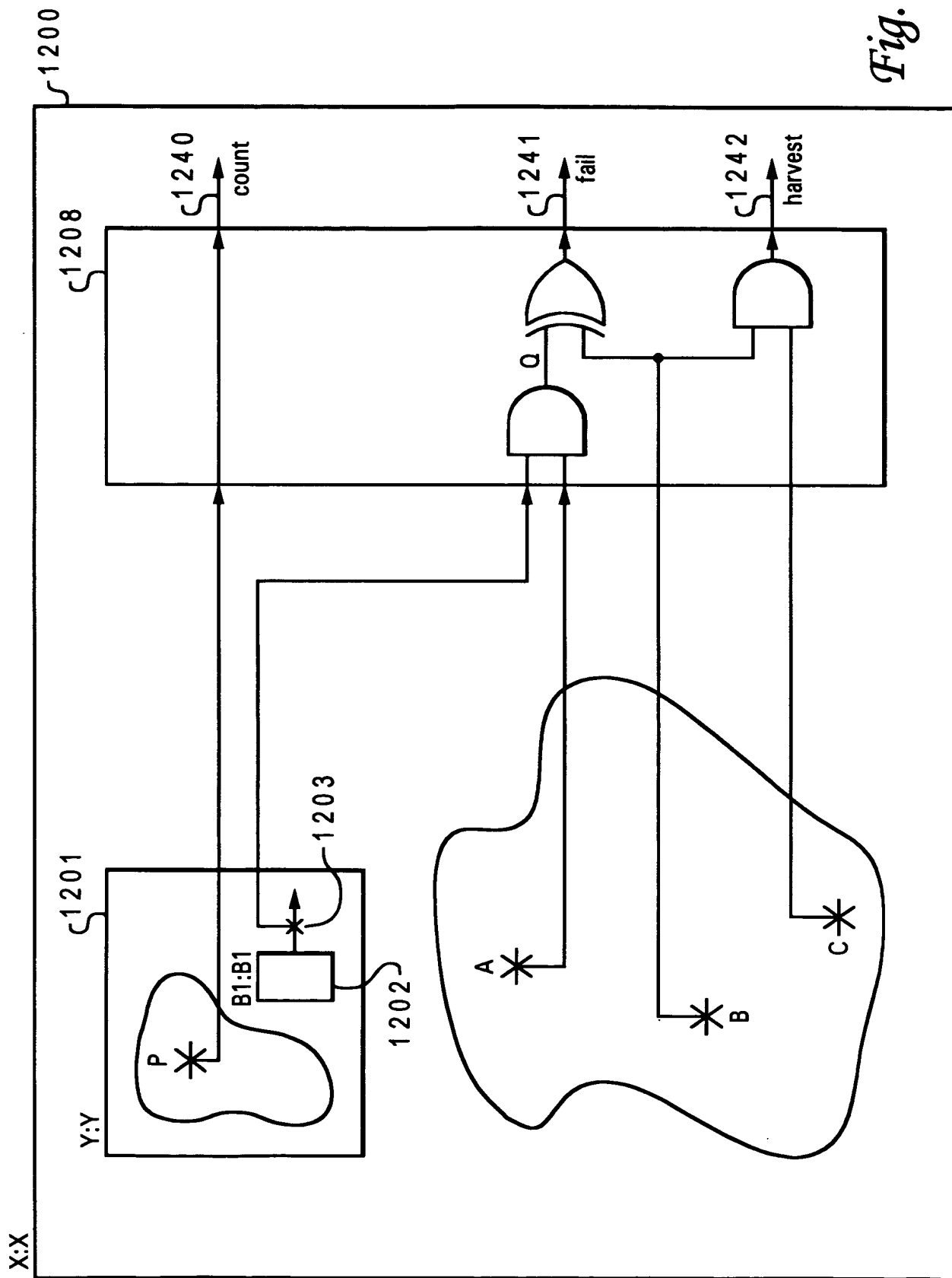
*Fig. 11B*

--!! Inputs  
--!! event\_1108\_in <= C.[count.event\_1108];  
--!! event\_1124\_in <= B.[count.event\_1124];  
--!! End Inputs

1171 }  
1172 }

*Fig. 11C*

T06070-2525260



```
PORT(      :
           :
           :
           :
           );
```

**BEGIN**

```

.
.
.
.
.
... HDL code for X ...
.
.
.
.
.

```

```

1 2 2 1 { Y:Y
          PORT MAP( :
                  );

```

$$1222 \left\{ \begin{array}{l} A \leq \dots \\ B \leq \dots \\ C \leq \dots \end{array} \right.$$

```

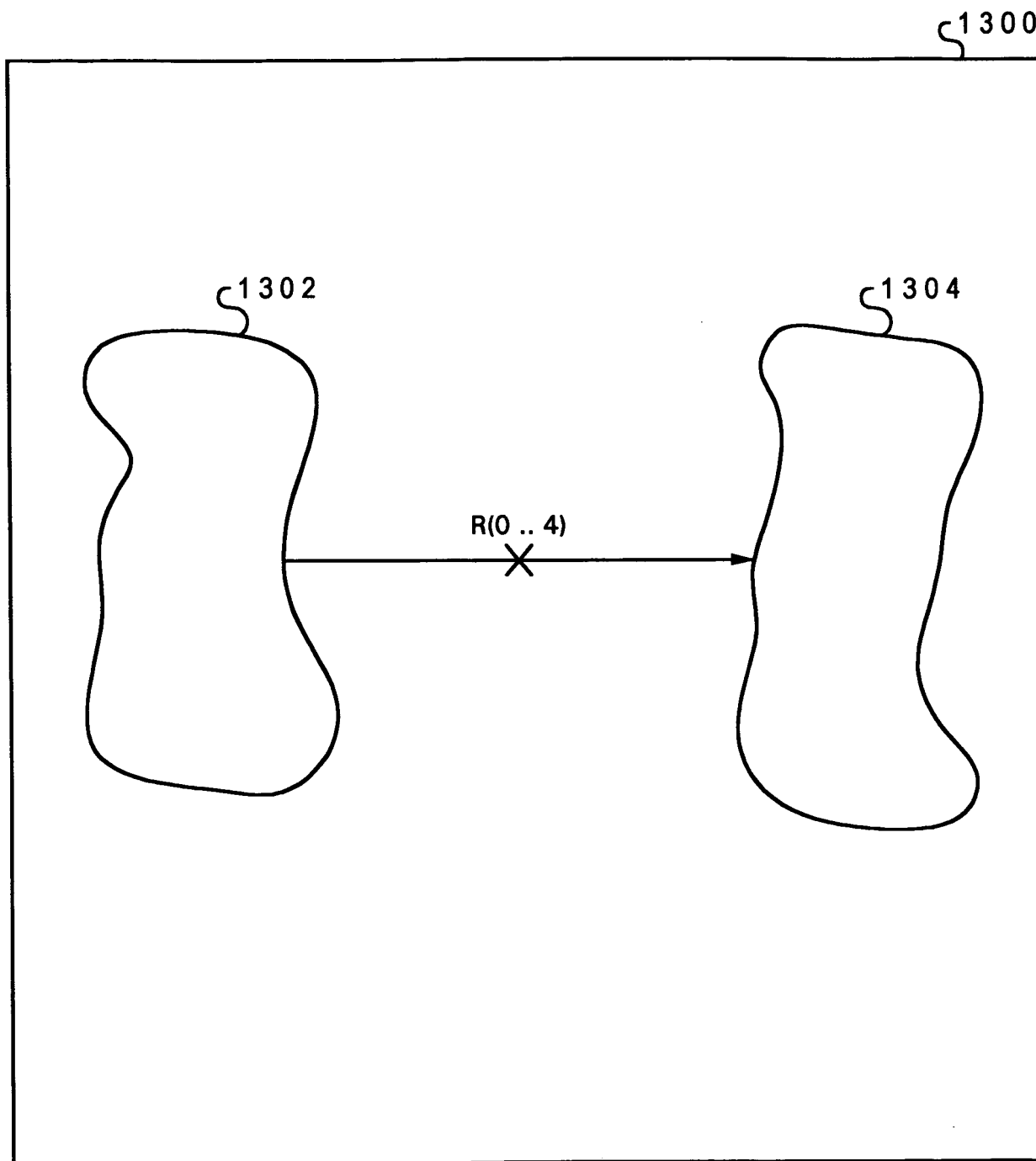
1 2 2 3 {
    C <= ....
    --!! [count, countname0, clock] <= Y.P;
    --!! Q <= Y. [B1.count.count1] AND A;
    --!! [fail, failname0, "fail msg"] <= Q XOR B;
    --!! [harvest, harvestname0, "harvest msg"] <= B AND C;
    END;

```

1220

*Fig. 12B*

[illegible]

*Fig. 13A*



FOO:FOO

1300

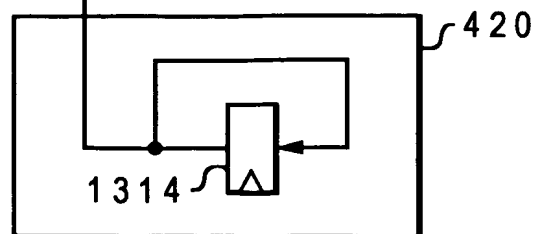
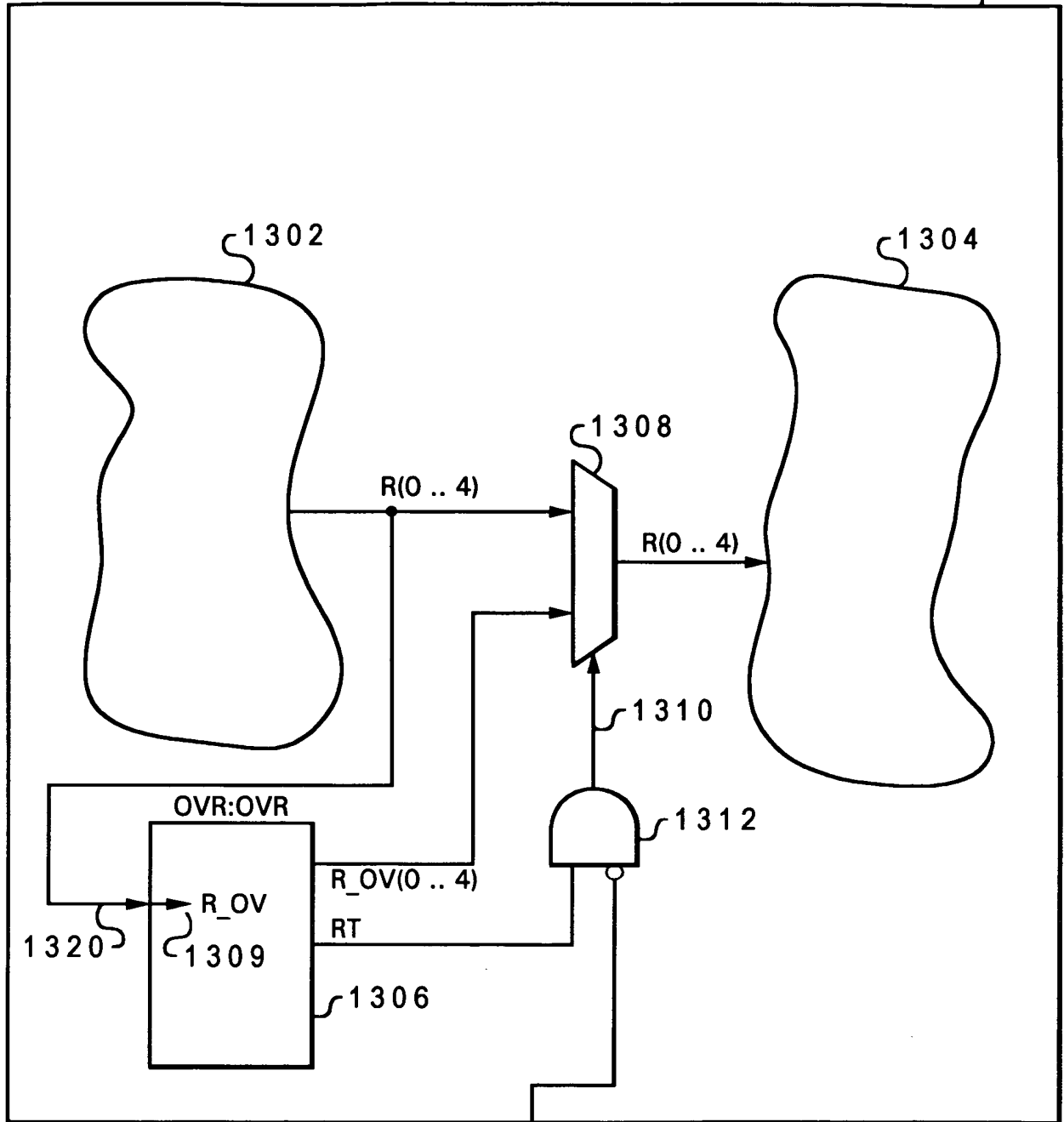


Fig. 13B

FOO:FOO 25225/60



ENTITY OVR IS

PORT( R\_IN : IN std\_ulogic\_vector(0 .. 4);

...

... other ports as required ...

...

R\_OV : OUT std\_ulogic\_vector(0 .. 4);

RT : OUT std\_ulogic

);

--!! BEGIN

--!! Design Entity: FOO;

--!! Inputs (0 to 4)

--!! R\_IN => {R(0 .. 4)};

--!! :

... other ports as needed ...

--!! :

--!! End Inputs

--!! Outputs

--!! <R\_OVRRIDE> : R\_OV(0 .. 4) => R(0 .. 4) [RT];

--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS

BEGIN

... HDL code for entity body section ...

END;

1364

1362

1363

1360

1361

1351

1356

1340

1358

Fig. 13C

T06040-2523260



ENTITY FOO IS

PORT( :  
:  
:  
);

ARCHITECTURE example of FOO IS

BEGIN

.  
.  
.  
.  
.  
R <= .....  
.  
.  
.  
.

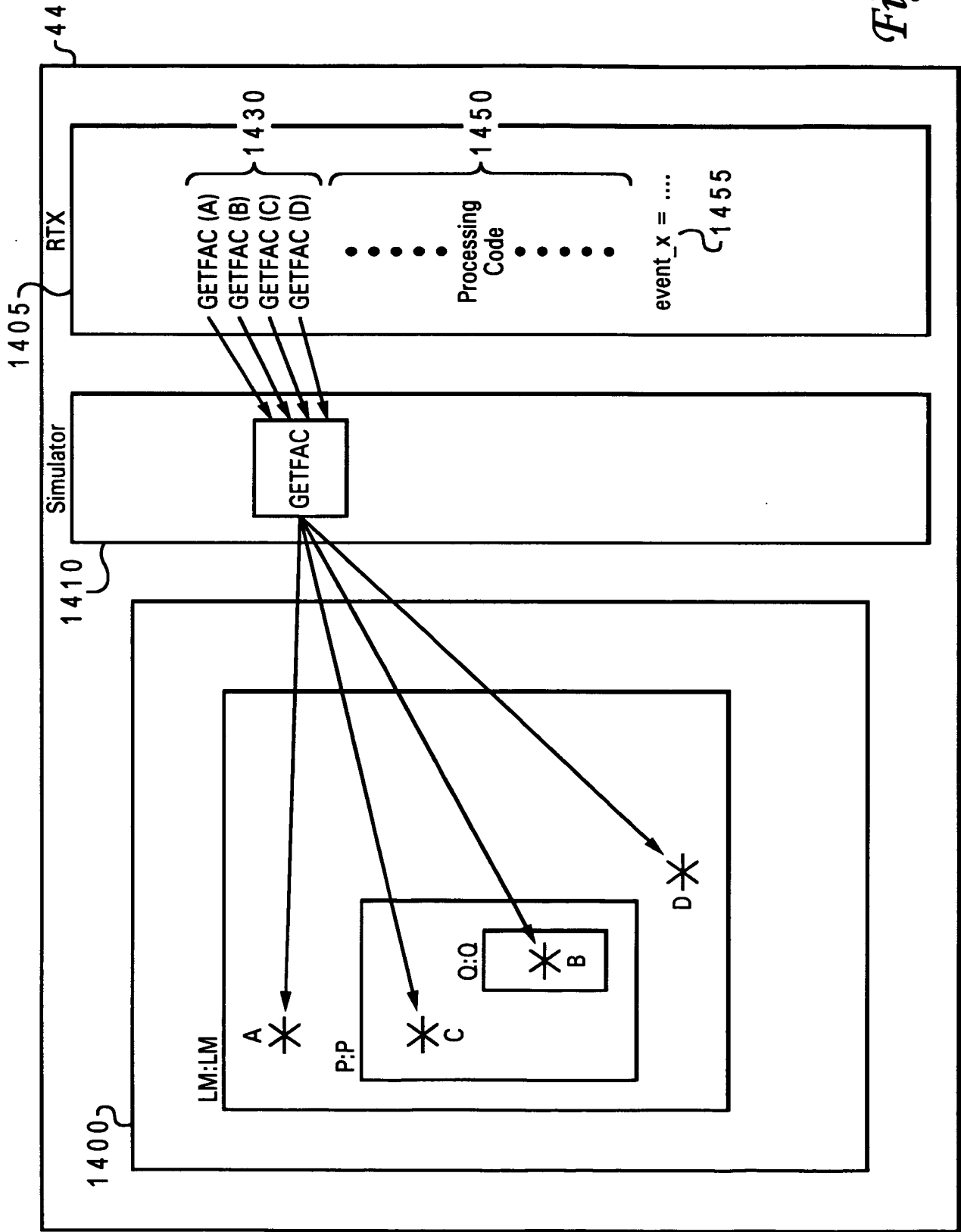
1380 { --!! R\_IN <= {R}; 1381  
--!! 1382  
--!!  
--!! R\_OV(0 to 4) <= .....; 1383  
--!! RT <= .....;  
--!! [override, R\_OVERRIDE, R(0 .. 4), RT] <= R\_OV(0 to 4); 1384

*Fig. 13D*

092225260



Fig. 14A



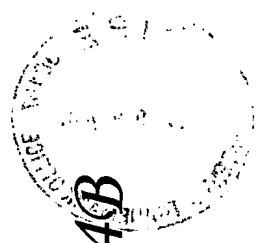
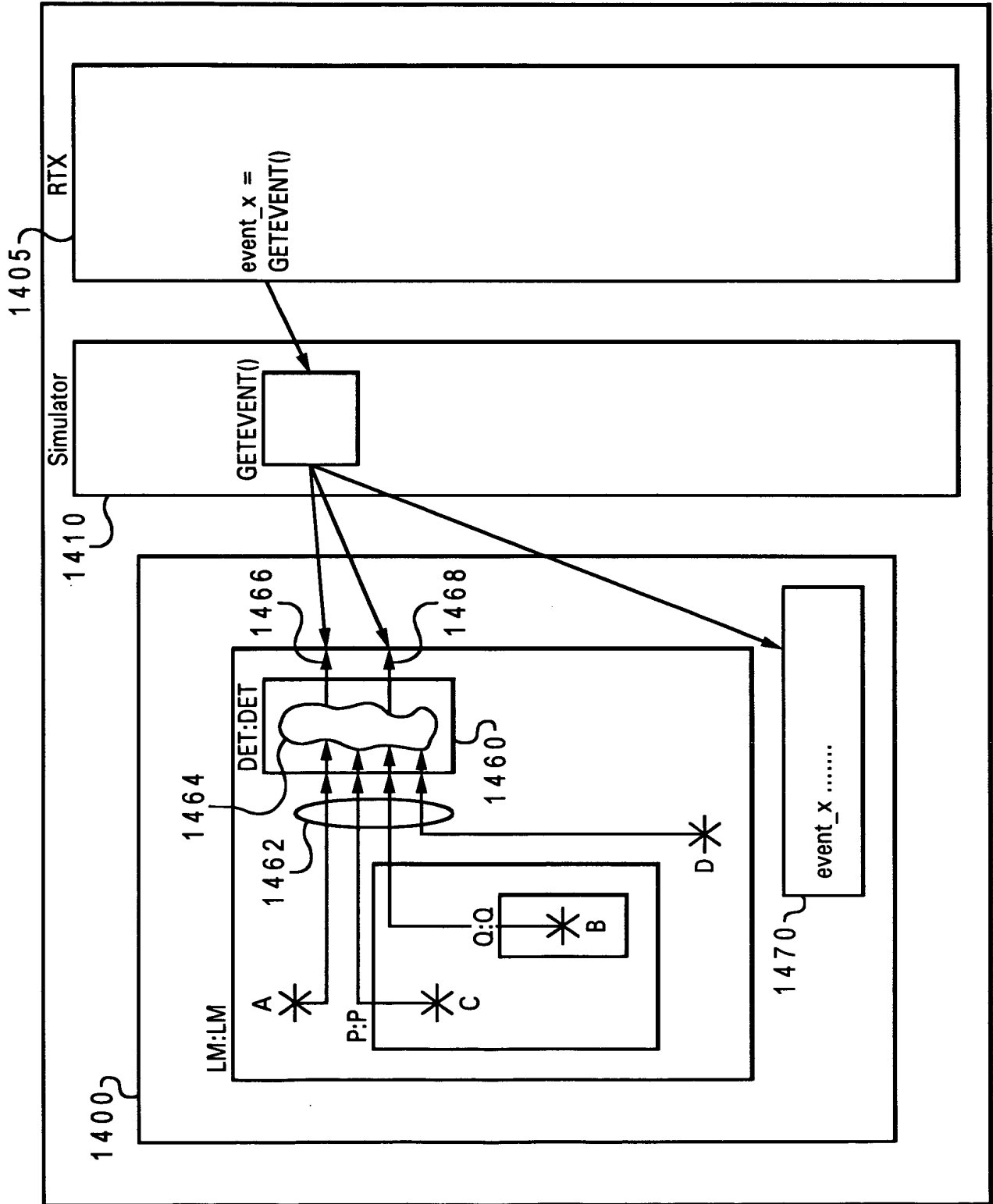


Fig. 14B





## ENTITY DET IS

```

PORT(  A      :  IN std_ulogic;
       B      :  IN std_ulogic_vector(0 to 5);
       C      :  IN std_ulogic;
       D      :  IN std_ulogic;
       :
       :
       event_x :  OUT std_ulogic_vector(0 to 2);
       x_here  :  OUT std_ulogic;
);

```

```

1491 { --!! BEGIN
      --!! Design Entity: LM;

      --!! Inputs
      --!! A  =>  A;
      --!! B  =>  P.Q.B;
      --!! C  =>  P.C;
      --!! D  =>  D;
      --!! End Inputs
      --!! Detections
      --!! <event_x>:event_x(0 to 2) [x_here];
      --!! End Detections
      --!! End;

1492 { ARCHITECTURE example of DET IS
      BEGIN
          ... HDL code ...
      END;

```

1493

1495

1494

1480

*Fig. 14C*